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Amplify the Human Experience

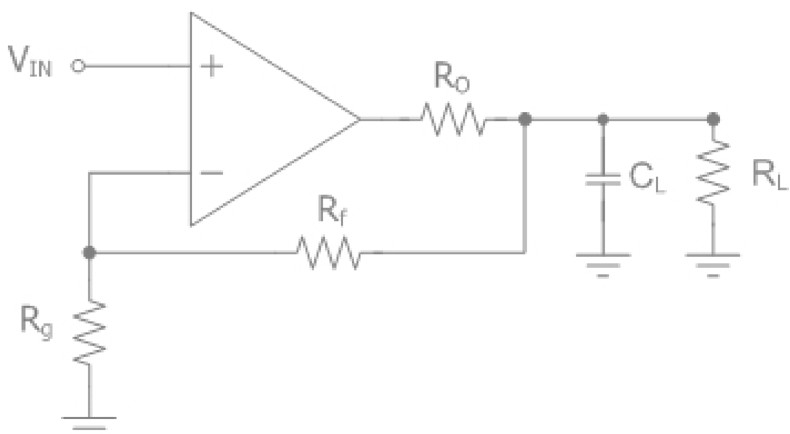
AN-2
Driving Capacitive Loads

Introduction

The load impedance that a capacitor presents to an amplifier decreases as the frequency increases. The frequency that matters here is not the applied signal frequency, but rather the frequency response of the amplifier used. High speed amplifiers are more sensitive to capacitive loading because the load impedance is lower (harder to drive) than for a lower speed amplifier. What this means is that layouts and loads you can get away with in a 1MHz bandwidth amplifier will often cause problems for a higher speed amplifier.

Why is driving a capacitor a problem?

Amplifiers have a non-zero output impedance. The output impedance, combined with the load capacitor and other components, puts an additional pole in the feedback loop.

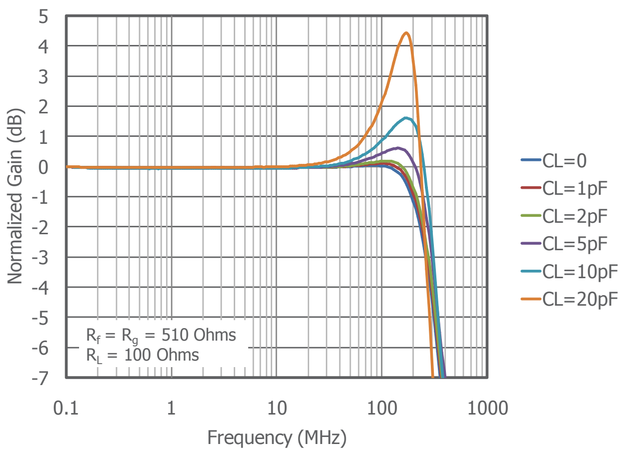


A pole is introduced corresponding to the capacitor time constant. This time constant is determined by the resistance seen by the capacitor—the parallel combination of R_O, R_L and (R_f+R_g). Moving the pole to higher frequency requires lowering one or more of the resistor values.

The new pole is in addition to the normal loop response of the amplifier. At best, it can seriously degrade phase margin, at worst it will cause oscillation. The situation can be improved by decreasing the value of R_L, but this can cause other problems with signal fidelity and power.

Example: CLC2600 with Capacitive Loading

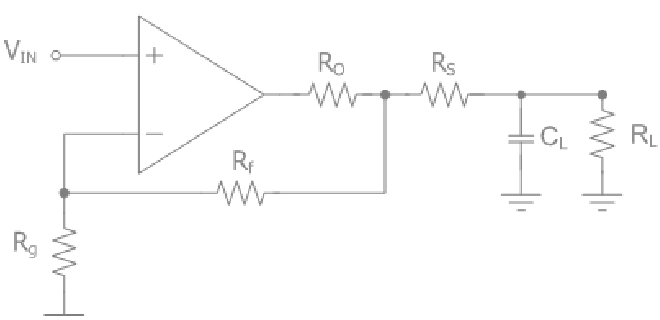
The plot below shows the effect of capacitive load on the CLC2600 op amp. These measurements use the same schematic as above (R_O is not an external component, it is internal to the amplifier), R_f=R_g=510 Ohms, R_L=100.



Increasing load capacitance causes increased peaking. Going much above 20pF will cause the amplifier to oscillate. If the load resistance is increased or removed, the peaking gets worse.

What can you do about it?

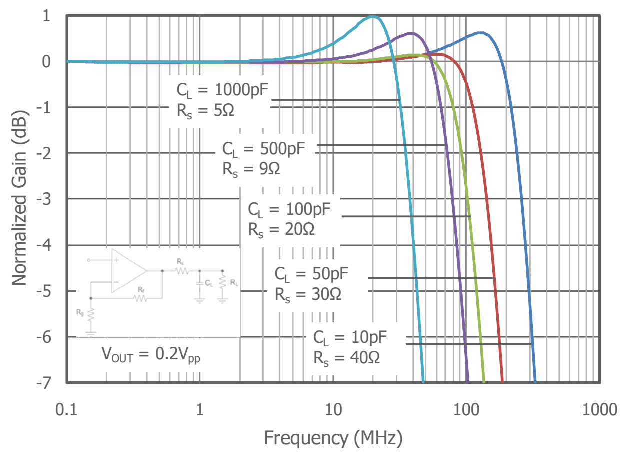
The best improvement can be had by reducing or removing the capacitive load, but this usually isn't a possibility. The easiest thing to do is to add a series resistor (R_S) between the op amp output and the load capacitor. At first this sounds like it might make matters worse, but this additional external resistance is outside the feedback loop instead of inside it:



Rs reduces the phase shift added by Cload, providing isolation between the amplifier and the load capacitance. Selecting the right value of Rs will control the peaking caused by the load capacitor with some reduction in bandwidth.

How well does it work?

R_S is selected in the CLC2600 data below by choosing the smallest value of resistor that keeps peaking below 1dB. The resistor values don't need to be exactly as shown—a little higher resistance will result in less peaking and a little less bandwidth.



Using the correct value of series resistor allows driving a wide range of load capacitor values. The series resistor value depends mostly on the amplifier bandwidth; check the amplifier product datasheet for value recommendations.

For additional information regarding our products, please visit CADEKA at: cadeka.com

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