Preliminary Data Sheet

CADEKA™
Amplify the Human Experience

Comlinear™ CLC2000

High Output Current Dual Amplifier

FEATURES

- 9.4V_{pp} output drive into R_L=25Ω
- Using both amplifiers, 18.8V_{pp} differential output drive into R_L=50Ω
- ±200mA @ V_O=9.4V_{pp}
- 0.009%/0.06° differential gain/phase error
- 250MHz -3dB bandwidth at G = 2
- 510MHz -3dB bandwidth at G = 1
- 210V/µs slew rate
- 4.5nV/√Hz input voltage noise
- 2.7pA/√Hz input voltage noise
- 7mA supply current
- Fully specified at ±5V supplies
- Lead-free SOIC-8 package

APPLICATIONS

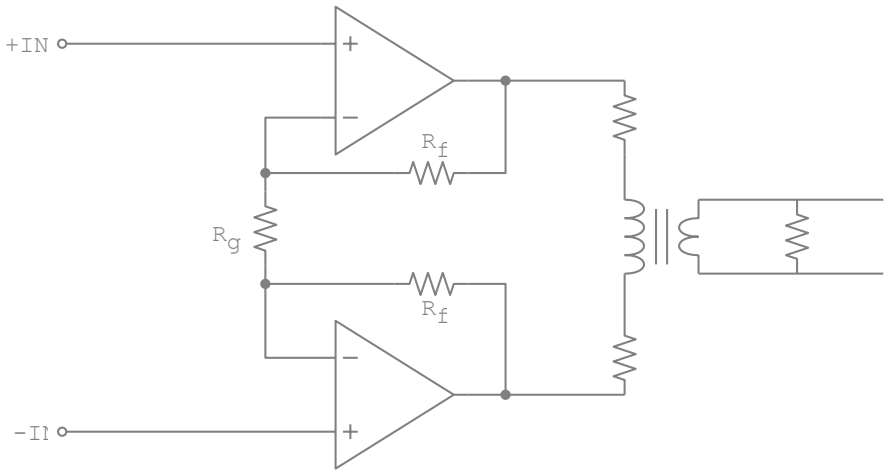
- ADSL PCI modem cards
- xDSL external modems
- Cable drivers
- Video line driver
- Twisted pair driver/receiver

General Description

The *Comlinear* CLC2000 is a dual voltage feedback amplifier that offers ±200mA of output current at 9.4V_{pp}. The CLC2000 is capable of driving signals to within 1V of the power rails. When connected as a differential line driver, the dual amplifier drives signals up to 18.8Vpp into a 25Ω load, which supports the peak upstream power levels for upstream full-rate ADSL applications.

The *Comlinear* CLC2000 can operate from single or dual supplies from 5V to 12V. It consumes only 7mA of supply current per channel. The combination of wide bandwidth, low noise, low distortion, and high output current capability makes the CLC2000 ideally suited for xDSL or video line driving applications.

Typical Application - ADSL Application

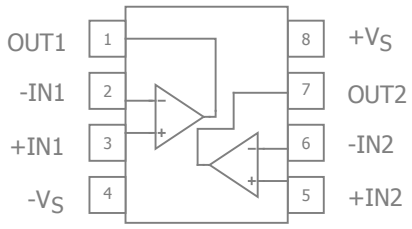


Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
CLC2000IM8X	SOIC-8	Yes	-40°C to +85°C	Reel
CLC2000IM8	SOIC-8	Yes	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.

CLC2000 Pin Configuration



CLC2000 Pin Assignments

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Package Thermal Resistance				
8-Lead SOIC		TBD		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOIC-8
Human Body Model (HBM)	4kV
Charged Device Model (CDM)	TBD

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	±2.5		±6.5	V

Electrical Characteristics

T_A = 25°C, V_S = ±2.5V, R_f = R_g = 510Ω, R_L = 100Ω, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}, R_L = 0		422		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		236		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		68		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		77		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 2V step; (10% to 90%)		3.7		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		tbd		ns
OS	Overshoot	V_{OUT} = 0.2V step		6		%
SR	Slew Rate	2V step		200		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-83		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-85		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-86		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-82		dBc
D_G	Differential Gain	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		tbd		%
D_P	Differential Phase	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		tbd		°
e_n	Input Voltage Noise	> 1MHz		4.2		nV/√Hz
i_n	Input Current Noise	> 1MHz		tbd		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz		-63		dB
DC Performance						
V_{IO}	Input Offset Voltage			0.3		mV
dV_{IO}	Average Drift			tbd		µV/°C
I_{IO}	Input Offset Current			0.2		µA
I_b	Input Bias Current			10		µA
dI_{bni}	Average Drift			tbd		nA/°C
PSRR	Power Supply Rejection Ratio	DC		81		dB
A_{OL}	Open-Loop Gain	R_L = 25Ω		76		dB
I_S	Supply Current	per channel		6.75		mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		tbd		MΩ
C_{IN}	Input Capacitance			tbd		pF
CMIR	Common Mode Input Range			±2.1		V
CMRR	Common Mode Rejection Ratio	DC		80		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		tbd		mΩ
V_{OUT}	Output Voltage Swing	R_L = 25Ω		±1.55		V
		R_L = 1kΩ		±1.75		V
I_{OUT}	Output Current			tbd		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		tbd		mA

Electrical Characteristics

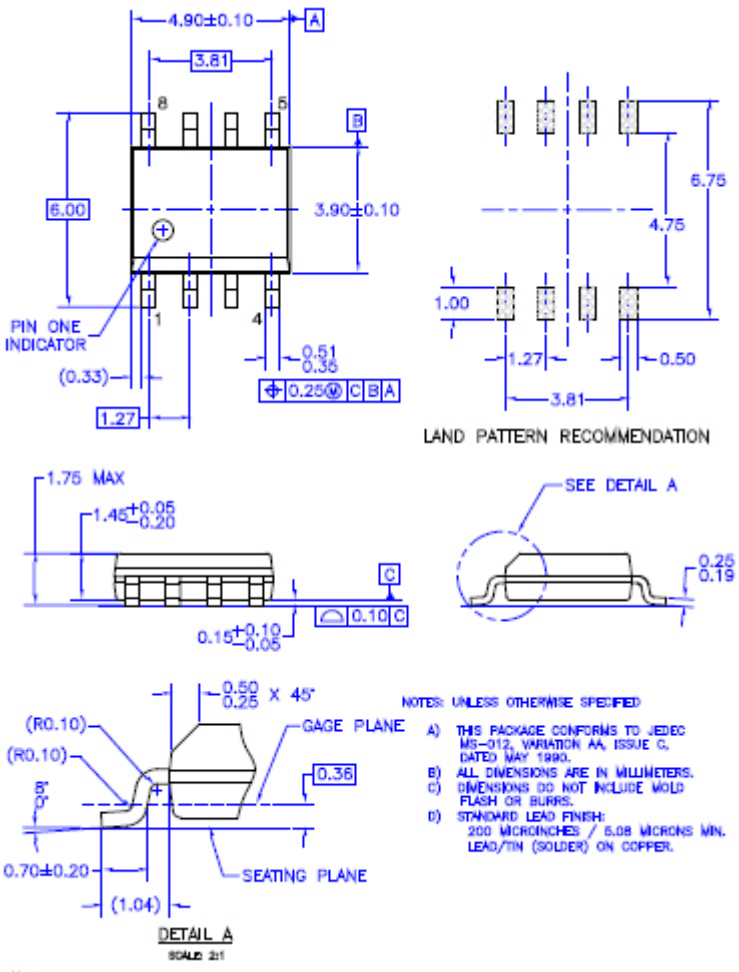
T_A = 25°C, V_S = ±6V, R_f = R_g = 510Ω, R_L = 100Ω, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}, R_L = 0		510		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		250		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 4V_{pp}		35		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		32		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 4V step; (10% to 90%)		13.3		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		tbd		ns
OS	Overshoot	V_{OUT} = 0.2V step		2		%
SR	Slew Rate	4V step		210		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-84		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-86		dBc
		8.4V_{pp}, 100KHz, R_L = 25Ω		-63		dBc
		8.4V_{pp}, 1MHz, R_L = 100Ω		-82		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-88		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-80		dBc
		8.4V_{pp}, 100KHz, R_L = 25Ω		-63		dBc
		8.4V_{pp}, 1MHz, R_L = 100Ω		-83		dBc
D_G	Differential Gain	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.009		%
D_P	Differential Phase	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.06		°
e_n	Input Voltage Noise	> 1MHz		4.5		nV/√Hz
i_n	Input Current Noise	> 1MHz		2.7		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz		-62		dB
DC Performance						
V_{IO}	Input Offset Voltage(1)		-4.2	0.3	4.2	mV
dV_{IO}	Average Drift			tbd		µV/°C
I_{IO}	Input Offset Current(1)		-2	0.2	2	µA
I_b	Input Bias Current(1)			10	20	µA
dI_{bni}	Average Drift			tbd		nA/°C
PSRR	Power Supply Rejection Ratio(1)	DC	73	81		dB
A_{OL}	Open-Loop Gain	R_L = 25		76		dB
I_S	Supply Current(1)	per channel		7	9	mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		tbd		MΩ
C_{IN}	Input Capacitance			tbd		pF
CMIR	Common Mode Input Range			±5.4		V
CMRR	Common Mode Rejection Ratio(1)	DC	70	79		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		tbd		mΩ
V_{OUT}	Output Voltage Swing	R_L = 25Ω (1)	-4.5	±4.8	4.5	V
		R_L = 1kΩ		±5.2		V
I_{OUT}	Output Current			tbd		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		1000		mA

Notes:
1. 100% tested at 25°C

Mechanical Dimensions

SOIC-8 Package



For additional information regarding our products, please visit the CADEKA at: cadeka.com

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